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Arm Solutions at Lightspeed

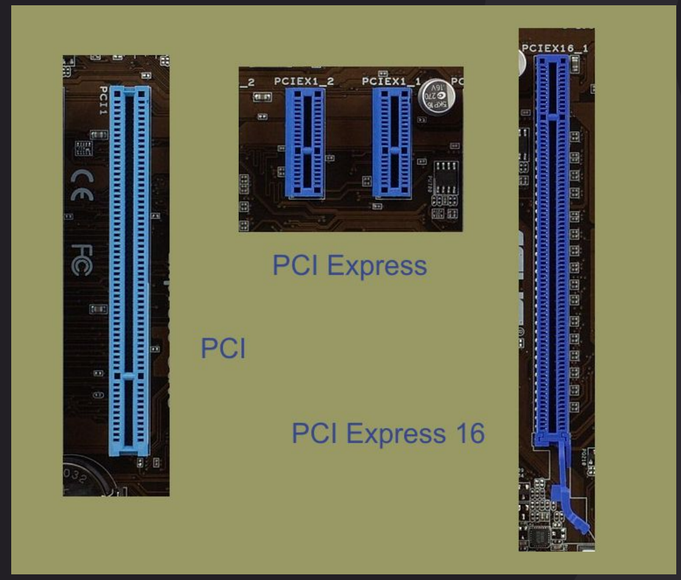
How (not) to write PCI(e) controller drivers in Linux Kernel

Manivannan Sadhasivam - Linaro

Why this talk?

PCIe in a Nutshell

- Peripheral Component Interconnect



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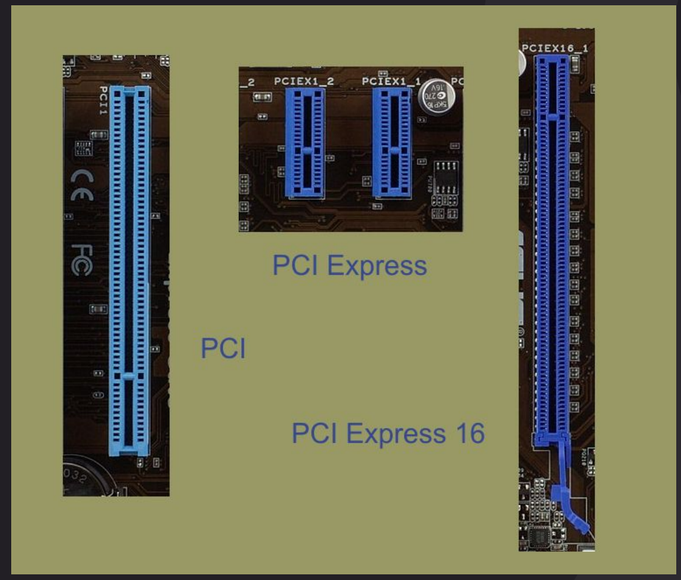

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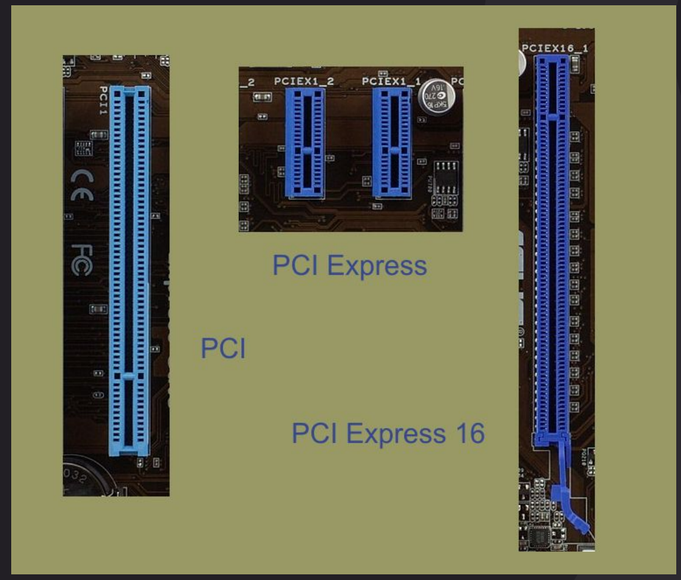

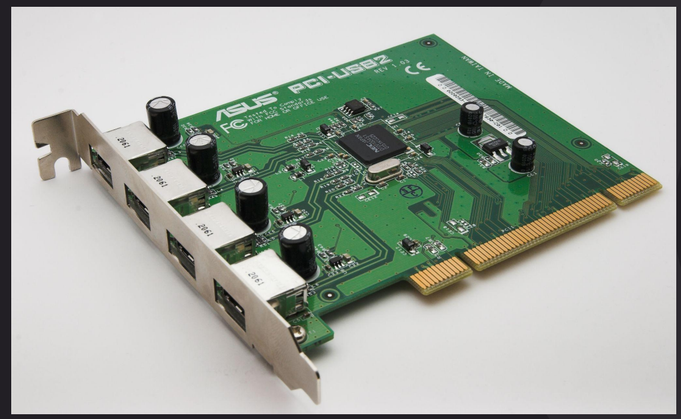

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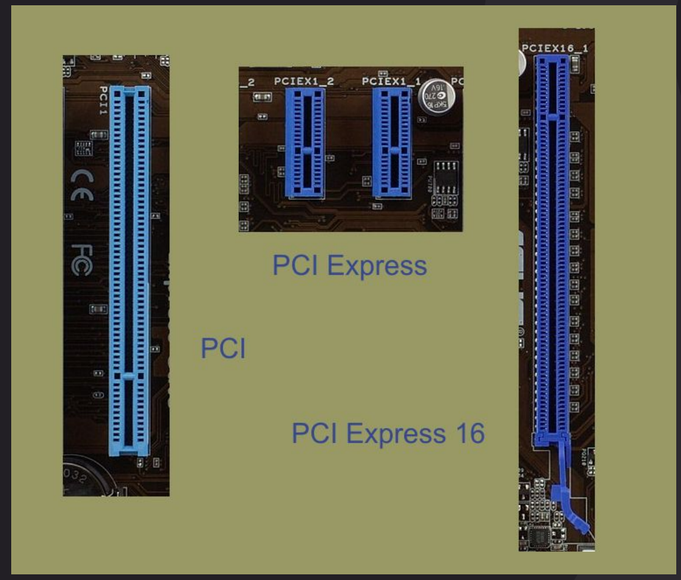

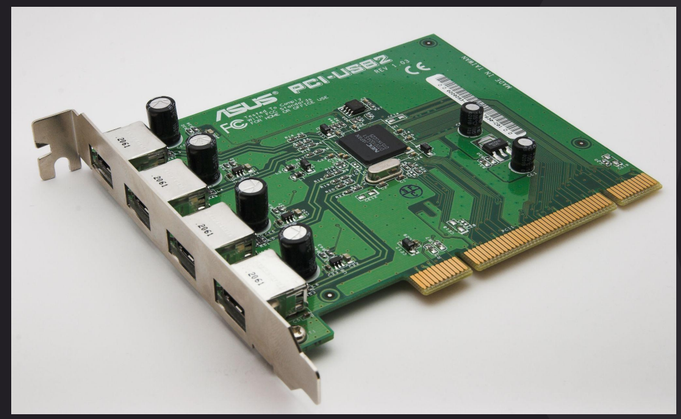

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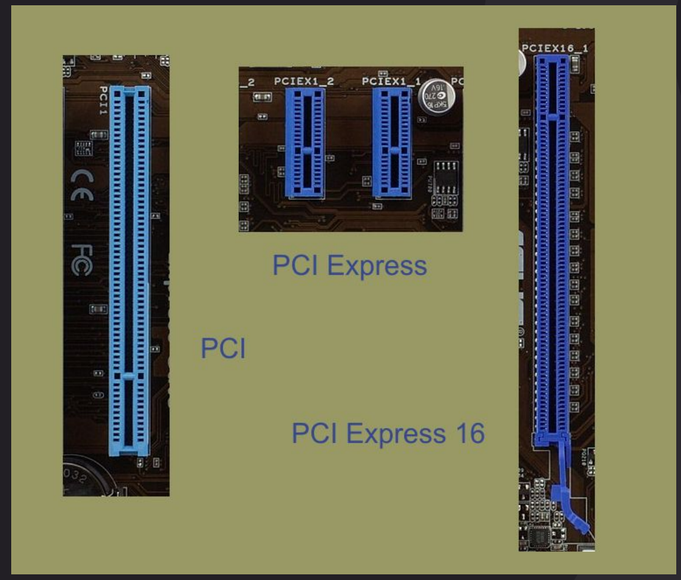

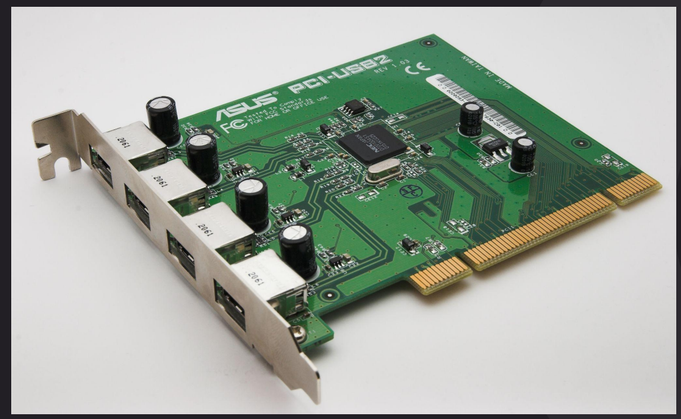

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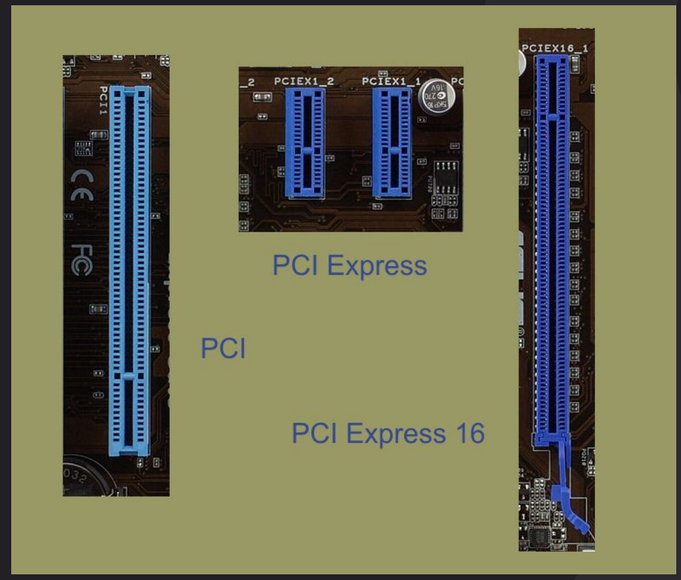

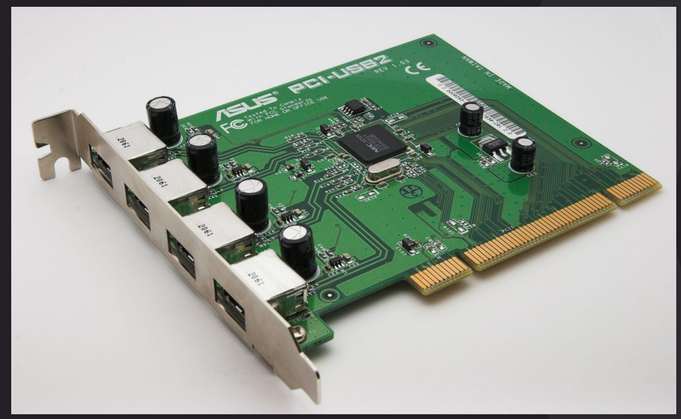

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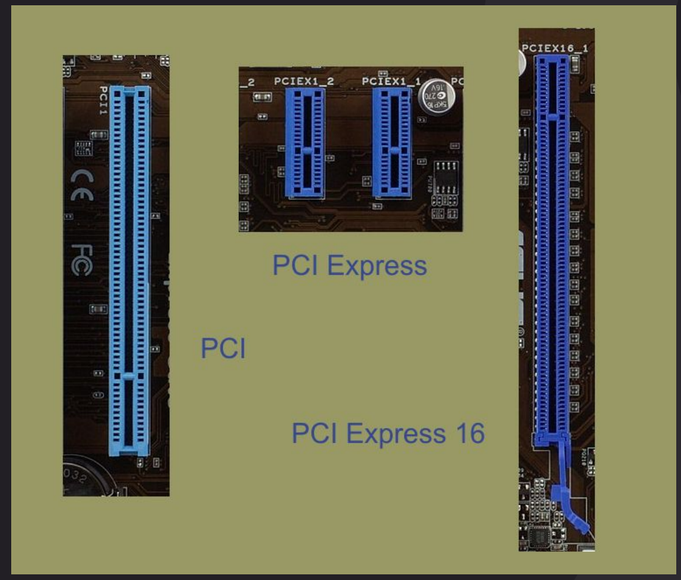
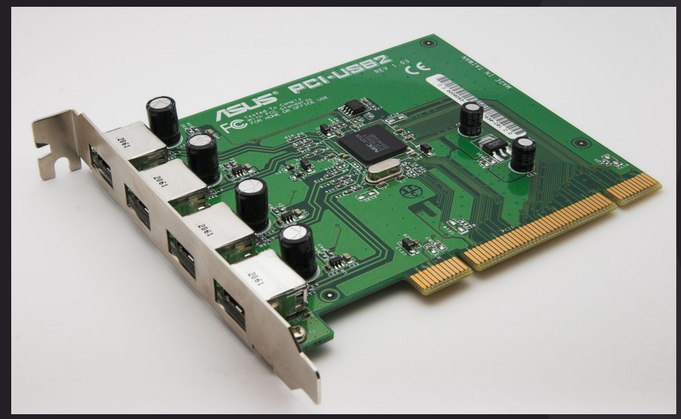
- Supports I/O Virtualization (SR-IOV)





PCIe Architecture

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- Point to Point topology
  - PCIe Root Complex - Host
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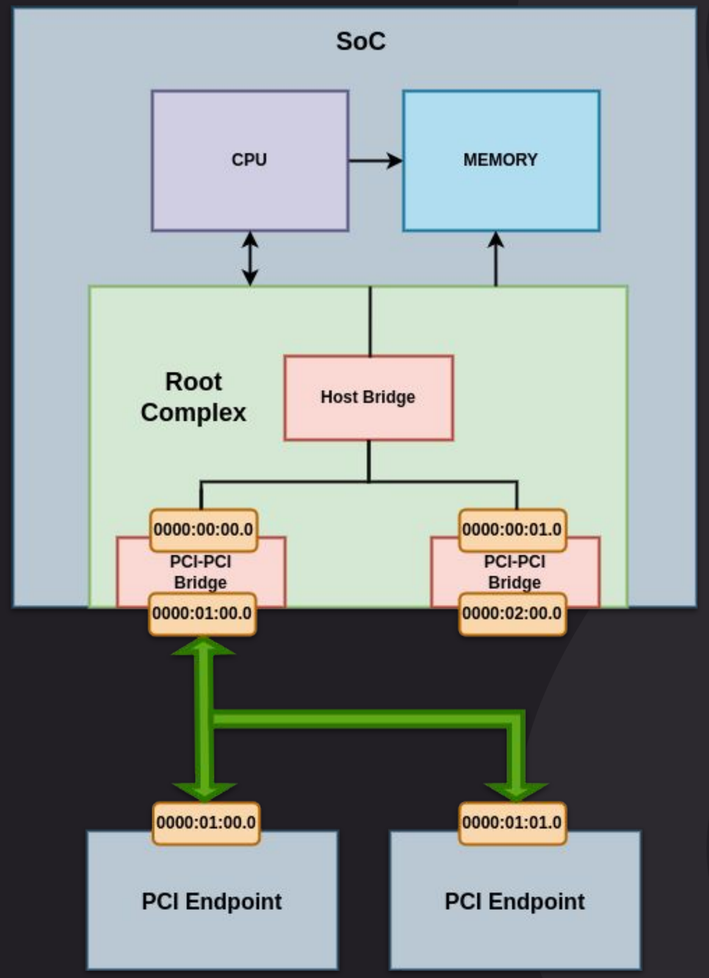

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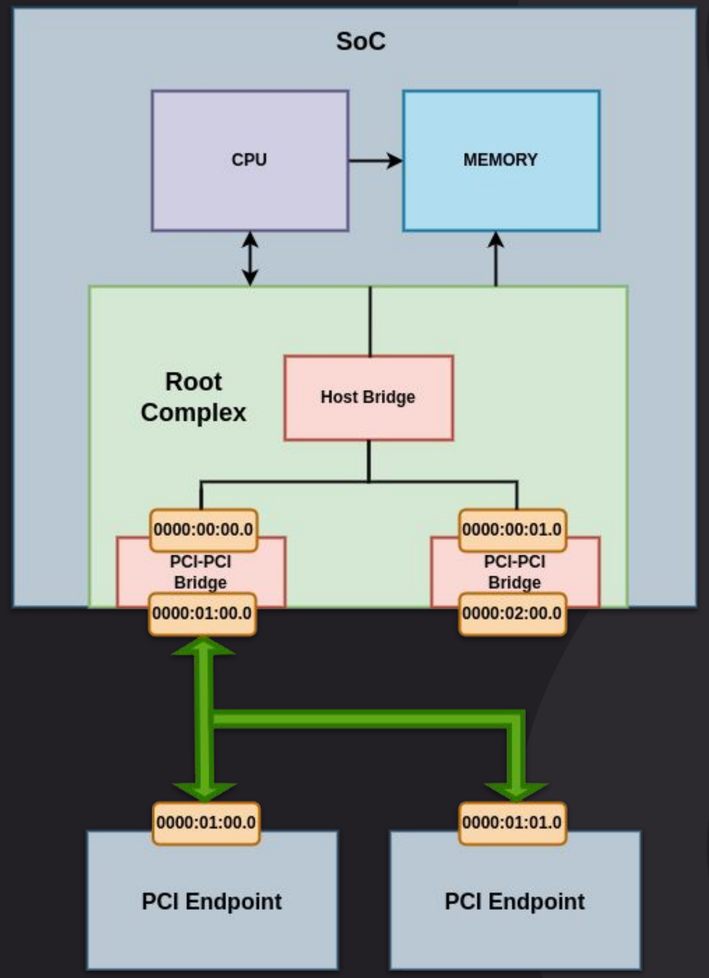
  - 8 bit Bus - 256 Busses
  - 5 bit Device - 32 Devices
  - 3 bit Function - 8 Functions



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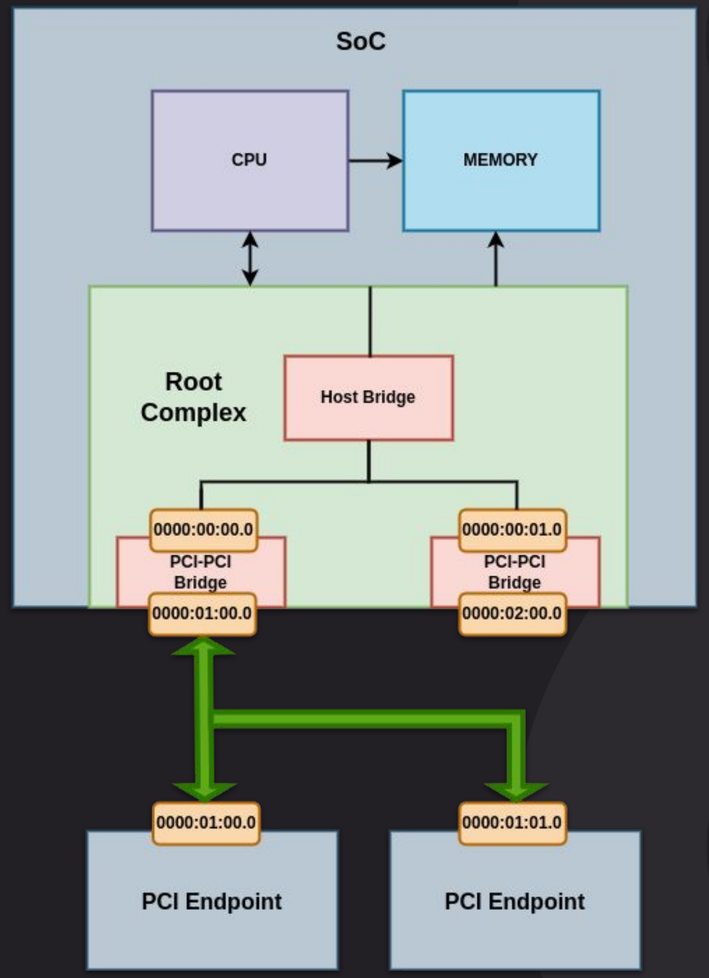
- PCIe Switches are often used for port expansion



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  - Setup MSI/MSI-X/INTx
  - Setup Address Translation Unit (ATU) for MEM/IO region
  - Setup DMA
  - Start LTSSM
  - Enumerate endpoint devices
    - pci_host_probe()

4 Common Mistakes & Solutions

Mistakes and Solutions

Mistake 1

Mistakes and Solutions

Mistake 1

- Root ports not described in firmware
    - Devicetree mostly

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- Controller node ends up hosting root port properties

```
pcie0: pcie@600000 {
        compatible = "qcom,pcie-sm8250";

        [...]

        iommu-map = <0x0   &apps_smmu 0x1c00 0x1>,
                    <0x100 &apps_smmu 0x1c01 0x1>;

        [...]

        phys = <&pciephy_0>;
        phy-names = "pciephy";

        [...]

        reset-gpios = <&tlmm 79 GPIO_ACTIVE_LOW>;
        wake-gpios = <&tlmm 81 GPIO_ACTIVE_HIGH>;

        [...]
};
```

Mistakes and Solutions

Solution

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Solution

- Move Root Port properties to Root Port

Mistakes and Solutions

Solution

- Move Root Port properties to Root Port

```
pcie0: pcie@600000 {
        compatible = "qcom,pcie-sm8250";

        [...]

        pcieport0: pcie@0 {
                device_type = "pci";
                reg = <0x0 0x0 0x0 0x0 0x0>;
                bus-range = <0x01 0xff>;

                #address-cells = <3>;
                #size-cells = <2>;
                ranges;

                iommu-map = <0x0   &apps_smmu 0x1c00 0x1>,
                            <0x100 &apps_smmu 0x1c01 0x1>;
                phys = <&pciephy_0>;
                phy-names = "pciephy";
                reset-gpios = <&tlmm 79 GPIO_ACTIVE_LOW>;
                wake-gpios = <&tlmm 81 GPIO_ACTIVE_HIGH>;
        };
};
```

Mistakes and Solutions

Mistake 2

Mistakes and Solutions

Mistake 2

- Slot/Endpoint power supplies defined in host bridge node

Mistakes and Solutions

Mistake 2

- Slot/Endpoint power supplies defined in host bridge node

```
pcie0: pcie@600000 {
        compatible = "qcom,pcie-sm8250";

        [...]
        vpcie12v-supply = <&pcie0_12v>;
        vpcie3v3-supply = <&pcie0_3p3v>;
        vpcie3v3aux-supply = <&pcie0_3p3v_aux>;
};
```

Mistakes and Solutions

Solution 1

Mistakes and Solutions

Solution 1

- Define slot supplies in Root Port node

Mistakes and Solutions

Solution 1

- Define slot supplies in Root Port node

```
pcie0: pcie@600000 {
        compatible = "qcom,pcie-sm8250";

        [...]

        pcieport0: pcie@0 {
                device_type = "pci";
                reg = <0x0 0x0 0x0 0x0 0x0>;
                bus-range = <0x01 0xff>;

                [...]

                vpcie12v-supply = <&pcie0_12v>;
                vpcie3v3-supply = <&pcie0_3p3v>;
                vpcie3v3aux-supply = <&pcie0_3p3v_aux>;
};
```

Mistakes and Solutions

Solution 1

- Define slot supplies in Root Port node
  - Rely on PWRCTRL drivers (CONFIG_PCI_PWRCTL*)
    - Works for standard supplies

```
pcie0: pcie@600000 {
        compatible = "qcom,pcie-sm8250";

        [...]

        pcieport0: pcie@0 {
                device_type = "pci";
                reg = <0x0 0x0 0x0 0x0 0x0>;
                bus-range = <0x01 0xff>;

                [...]

                vpcie12v-supply = <&pcie0_12v>;
                vpcie3v3-supply = <&pcie0_3p3v>;
                vpcie3v3aux-supply = <&pcie0_3p3v_aux>;
};
```

Mistakes and Solutions

Solution 2

Mistakes and Solutions

Solution 2

- Define Endpoint supplies in Endpoint node

Mistakes and Solutions

Solution 2

- Define Endpoint supplies in Endpoint node

```
pcie0: pcie@600000 {
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        [...]

        pcieport0: pcie@0 {
                device_type = "pci";
                reg = <0x0 0x0 0x0 0x0 0x0>;
                bus-range = <0x01 0xff>;

                [...]

        wifi@0 {
                compatible = "pci17cb,1101";
                reg = <0x10000 0x0 0x0 0x0 0x0>;

                vddrfacmn-supply = <&vreg_pmu_rfa_cmn>;
                vddaon-supply = <&vreg_pmu_aon_0p59>;
                vddwlcx-supply = <&vreg_pmu_wlcx_0p8>;
                vddwlmx-supply = <&vreg_pmu_wlmx_0p85>;
                vddrfa0p8-supply = <&vreg_pmu_rfa_0p8>;
                vddrfa1p2-supply = <&vreg_pmu_rfa_1p2>;
                vddrfa1p7-supply = <&vreg_pmu_rfa_1p7>;
                vddpcie0p9-supply = <&vreg_pmu_pcie_0p9>;
                vddpcie1p8-supply = <&vreg_pmu_pcie_1p8>;
        };
};
```

Mistakes and Solutions

Solution 2

- Define Endpoint supplies in Endpoint node
  - Rely on PWRSEQ drivers (CONFIG_PCI_PWRCTL_PWRSEQ/CONFIG_POWER_SEQUENCING*)
    - Works for complex supplies

```
pcie0: pcie@600000 {
        compatible = "qcom,pcie-sm8250";

        [...]

        pcieport0: pcie@0 {
                device_type = "pci";
                reg = <0x0 0x0 0x0 0x0 0x0>;
                bus-range = <0x01 0xff>;

                [...]

        wifi@0 {
                compatible = "pci17cb,1101";
                reg = <0x10000 0x0 0x0 0x0 0x0>;

                vddrfacmn-supply = <&vreg_pmu_rfa_cmn>;
                vddaon-supply = <&vreg_pmu_aon_0p59>;
                vddwlcx-supply = <&vreg_pmu_wlcx_0p8>;
                vddwlmx-supply = <&vreg_pmu_wlmx_0p85>;
                vddrfa0p8-supply = <&vreg_pmu_rfa_0p8>;
                vddrfa1p2-supply = <&vreg_pmu_rfa_1p2>;
                vddrfa1p7-supply = <&vreg_pmu_rfa_1p7>;
                vddpcie0p9-supply = <&vreg_pmu_pcie_0p9>;
                vddpcie1p8-supply = <&vreg_pmu_pcie_1p8>;
        };
};
```

Mistakes and Solutions

Mistake 3

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Mistake 3

- Mapping each Outbound translation using ATU

Mistakes and Solutions

Mistake 3

- Mapping each Outbound translation using ATU

```
static void __iomem *dw_pcie_other_conf_map_bus(struct pci_bus *bus,
                                                unsigned int devfn, int where)
{
        struct dw_pcie_rp *pp = bus->sysdata;
        struct dw_pcie *pci = to_dw_pcie_from_pp(pp);
        struct dw_pcie_ob_atu_cfg atu = { 0 };
        int type, ret;
        u32 busdev;

        [...]

        ret = dw_pcie_prog_outbound_atu(pci, &atu);
        if (ret)
                return NULL;

        return pp->va_cfg0_base + where;
}

[...]

static struct pci_ops dw_child_pcie_ops = {
        .map_bus = dw_pcie_other_conf_map_bus,

        [...]
};
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Mistakes and Solutions

Mistake 3

- Mapping each Outbound translation using ATU
  - Inefficient and adds latency

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static void __iomem *dw_pcie_other_conf_map_bus(struct pci_bus *bus,
                                                unsigned int devfn, int where)
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        struct dw_pcie_rp *pp = bus->sysdata;
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Solution 1

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Solution 1

- Configure ECAM mode in bootloader

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- Configure ECAM mode in bootloader
- Pros
  - Ability to reuse existing controller drivers
    - pci-host-generic.c

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- Configure ECAM mode in bootloader
- Pros
  - Ability to reuse existing controller drivers
    - pci-host-generic.c
- Downside
  - Requires firmware change
  - Cannot reset the host bridge

Mistakes and Solutions

Solution 2

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Solution 2

- Configure ECAM mode in controller driver
  - Reference

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- Configure ECAM mode in controller driver
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  - Control lies with Linux Kernel
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- Configure ECAM mode in controller driver
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- Pros
  - Control lies with Linux Kernel
  - Can reset the host bridge
- Downside
  - Requires a separate controller driver

Mistakes and Solutions

Mistake 4

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Mistake 4

- shutdown() callback often not defined

Mistakes and Solutions

Mistake 4

- shutdown() callback often not defined
    - Developers get confused with remove()

Mistakes and Solutions

Mistake 4

- shutdown() callback often not defined
  - Developers get confused with remove()
  - Messes up endpoint state machine during warm reboot

Mistakes and Solutions

Solution

Mistakes and Solutions

Solution

- Define shutdown() callback

Mistakes and Solutions

Solution

- Define shutdown() callback
    - Put the endpoint into D3Cold

Mistakes and Solutions

Solution

- Define shutdown() callback
  - Put the endpoint into D3Cold
  - Send PME_Turn_Off

Mistakes and Solutions

Solution

- Define shutdown() callback
  - Put the endpoint into D3Cold
  - Send PME_Turn_Off
  - Wait for PME_TO_Ack from endpoint

Mistakes and Solutions

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- Define shutdown() callback
  - Put the endpoint into D3Cold
  - Send PME_Turn_Off
  - Wait for PME_TO_Ack from endpoint
  - Assert PERST#

Mistakes and Solutions

Solution

- Define shutdown() callback
  - Put the endpoint into D3Cold
  - Send PME_Turn_Off
  - Wait for PME_TO_Ack from endpoint
  - Assert PERST#
  - Remove power
    - Let the PWRCTRL driver take care of it!

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linaro.org

Thank you

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